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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,342	ANAND, ANUPAM	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/726,342, the examiner acknowledges the applicant's submission of the amendment dated 12/8/2008. At this point, claims 16-23 and 28-40 stand cancelled. Claims 1-15 and 24-27 are pending.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claim 24** is rejected under 35 U.S.C. 102(b) as being anticipated by Goldberg (US 6,874,062).

4. As per **claim 24**, Goldberg discloses a method for managing memory, the method comprising: analyzing a state of a first logic circuit to determine whether a block of memory segments includes a memory segment that is available for data storage, the first logic circuit having a first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; and if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage **[Goldberg discloses this limitation as "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources**

of Data Processing System" (Col. 7, lines 11-13) wherein "in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments… these Segments all include a same predetermined number of bits… a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB… indicating the availability of memory… a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory… a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) and explains performing "a search for an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text)].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-15 and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437).

7. As per **claims 1 and 25**, Goldberg discloses

A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage **["in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments… these Segments all include a same predetermined number of bits… a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB… indicating the availability of memory… a bit in Bitmap 1, is set to**

"0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory… a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)].

wherein the first state includes at least a portion of a memory address of the first memory block **[Goldberg discloses "in step 814 processing is completed and the memory address associated with the located available memory sections may be returned to the requested" (Col. 12, line 26-29) and discloses "a data structure that may be used to store the Hierarchical Bitmap Structure of the current invention… a level descriptor for each of the individual bitmaps in the Bitmap Packet 1002. This level descriptor includes information such as the starting address and bit-length of the corresponding bitmap" (Col. 15, lines 19-40; Figure 10 and related text)]**.

Goldberd does not explicitly disclose the details of having the first state include at least a portion of a memory address of the first memory block.

Lehman discloses having the first state includes at least a portion of a memory address of the first memory block as **["The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30… the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address… the**

bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array… For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text) and explains "FIG. 9 shows an allocation array that includes 5 groups of bitmaps each having 16 bits... there are 16 bits in a group, each having 16 address locations numbered 0-15" (col. 10, lines 50-60)]; therefore, bits which represent a first state and indicate availability of a memory block correspond to bits having "a first state" wherein since the bit position of these bits has a memory address, thus, the first state inherently includes at least a portion of a memory address of the memory block having available memory, as claimed. Note that the bits representing a first state in Lehman have a direct correspondence with their calculated memory address, thereby, *"including/comprising"* at least a portion of their memory address].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further

the first state includes at least a portion of a memory address of the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**"a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)**].

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 1 and 25.

8. As per **claim 2**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage [**Goldberg discloses "in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7… a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)**].

9. As per **claim 3**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, wherein the second state is a state of a single logic bit [**Goldberg discloses "a bit is set if a Section is in use and is cleared if the Section is available for**

allocation" (Col. 7, lines 50-61). Lehman also discloses this limitation, as a bit is 1 to represent allocated memory (See Figure 9 and related text) which corresponds to a second state].

10. As per **claim 4**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 1 wherein the second state comprises information of an offset to a next available memory block or memory segment **[Goldberg discloses "by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently" (Col. 10, lines 25-29). Lehman discloses "pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory]**.

11. As per **claim 5**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory

segment is not available for data storage **[Goldberg discloses "in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7… a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created… bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

12. As per **claim 6**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 2, wherein the first state of the second logic circuit comprises at least a portion of a memory address of the first memory segment **[Lehman discloses "The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30… the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address… the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array… For example, for size=1, the pattern 1100 1111 0011**

0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text); therefore, having bits which represent a first state which indicates availability of a memory block comprise *at least a portion* of a memory address of a memory block as the bit position indicating available memory indicates the address/position/location of the available memory block].

13. As per **claim 7**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, and explains **[Goldberg discloses this limitation as in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7… a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created… bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues… If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state… the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)]** Lehman discloses a third logic circuit that converts the first state of the first logic circuit and the first state

of the second logic circuit to the memory address of the first memory segment as [**"blocks larger than 1 can start only on an appropriate block address… the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)**].

14. As per **claim 8**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a plurality of logic bits and the first and second states of the second logic circuit are states of a plurality of digital bits **[Lehman discloses "the second type of allocation bit map, where size=0, is used for blocks that are sixteen times the unit size, or larger… In the second type bit map, the first byte is the status byte for the buddy segment" (Col. 11, lines 47-57); therefore, having a plurality of bits representing states/status]**.

15. As per **claim 9**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, wherein the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment **[Goldberg discloses this limitation as in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond**

to an associated one of Sections 0 trough 7… a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created… bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues… If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state… the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)].

16. As per **claims 10 and 26**, Goldberg discloses a memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; **["in a hierarchical bitmap**

scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments… these Segments all include a same predetermined number of bits… a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB… indicating the availability of memory… a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory… a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)]

wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block **[With respect to this limitation, Goldberg discloses "a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation" (Col. 8, line 23-32)]** but does not expressly disclose the details of wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block.

Lehman discloses wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block as [**"for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided" (Col. 11, lines 6-14)**].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further the first state comprise information indicating a number of available memory segments in the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**"a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)**].

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 10 and 26.

17. As per **claim 11**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 10, further comprising: a second logic circuit having a first state

when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; **["in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7… a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created… bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

18. As per **claim 12**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 11, wherein the first and second states of the second logic circuit are single-bit logic states **[The rationale in the rejection of claim 3 is herein incorporated]**.

19. As per **claims 13-15 and 27**, Goldberg discloses a memory management system for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising: a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; **["in a hierarchical bitmap scheme… the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8,**

lines 43-48) and explains "the LLB may be divided into Segments… these Segments all include a same predetermined number of bits… a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB… indicating the availability of memory… a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory… a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)]. wherein the second state of the first logic circuit comprise information indicating an offset to available memory **[Goldberg discloses "by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently" (Col. 10, lines 25-29)]** but doesn't expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory.

Lehman discloses the second state of the first logic circuit comprise information indicating an offset to available memory as **["pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free**

buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further specifically have the second state of the first logic circuit comprise information indicating an offset to available memory as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**"a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)**].

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 13-15 and 27.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

20. Applicant's arguments filed on 12/8/2008 with respect to 35 USC 112, first paragraph rejection of claims 1-15 and 25-27 have been fully considered and are deemed persuasive, as a result the 35 USC 112, first paragraph rejection of claims 1-15 and 25-27 are herein withdrawn.

21. Applicant's arguments filed on 12/8/2008 with respect to prior art obviousness type rejections of claims 1-15 and 24-27 have been fully considered but they are not deemed persuasive.

22. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

23. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

FIRST POINT OF ARGUMENT

24. Regarding Applicant's remark that the combination of Goldberg and Lehman does not disclose "the first state comprises at least a portion of a memory address of the first memory block" as Lehman discloses determining the address of a block based on bit position in the base group but does not disclose that "a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;" the Examiner respectfully disagrees.

According to Applicant's arguments, it appears that Applicant is reading the claims narrower than they are presented wherein the limitation "a first state of a logic circuit associated

with the first memory block comprising at least a portion of the memory address" has been interpreted according to the broadest reasonable interpretation given to the claims by one of ordinary skill in the art [See MPEP 2111].

Applicant should note that the combination of Goldberg and Lehman discloses "a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;" as Lehman discloses [**"The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30… the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address… the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array… For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text) where Lehman further explains "FIG. 9 shows an allocation array that includes 5 groups of bitmaps each having 16 bits... there are 16 bits in a group, <u>each having 16 address locations numbered 0-15</u>" (col. 10, lines 50-60)**]. Therefore, having bits which represent a first state which indicates availability of a memory

block comprise *at least a portion* of a memory address of a memory block as the bit position having a state indicating available memory has/comprises the address/position/location of the available memory block.

Furthermore, Applicant's specification recites **["the address-determining step 1040 may be accomplished in a variety of ways. For example, various information may be contained in the segment or block flags that the step 1040 may utilize to calculate segment address" (Specification, par. 96)]** wherein Applicant should note that this recitation does not distinguish Applicant's invention from the combination of Goldberg and Lehman since Lehman describes determining address portions of memory segments based on the position of the identified available bits (See above), wherein, the bits identifying available memory can be said to contain information that is utilized to calculate the segment's address, since the position of these bits comprises information inherently contained in said bits.

25. Applicant further argues "Lehman's bit position is not at least a portion of a memory address" and "although Lehman teaches that the address of a block is determined by the bit position, the bit position itself is not at least a portion of the memory address"; however, Lehman clearly discloses **["FIG. 9 shows an allocation array that includes 5 groups of bitmaps each having 16 bits... there are 16 bits in a group, <u>each having 16 address locations numbered 0-15</u>" (col. 10, lines 50-60)]** therefore, bits which represent a first state and indicate availability of a memory block correspond to bits having "a first state" wherein since the bit position of these bits has a memory address; these bits *"include/comprise"* at least a portion of their memory address.

<u>SECOND POINT OF ARGUMENT</u>

26. Regarding Applicant's remark that Goldberg teaches away from the combination with Lehman as Goldberg teaches away from using multiple bits representations since "Goldberg clearly criticizes, discredits and otherwise discourages optimizing memory allocation using multiple buffer pools as taught by Lehman" as Goldberg "explicitly states that the use of multiple buffer pools as taught by Lehman "results in a considerable waste of storage space" (Goldberg, Column 2, Lines 34-35). One of ordinary skill in the art, upon reading Goldberg would be discouraged from using multiple buffer pools to optimize memory allocation as taught by Lehman".

In response, these arguments have been fully considered but it is not deemed persuasive.

In view of the following discussion, Examiner would like to emphasize the following:

Sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent. The CCPA has held that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968); MPEP 2144.01.

In determining obviousness under 35 U.S.C. 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that: "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the Court states that "the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention…and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense".

In response to applicant's argument that Goldberg teaches away from its combination with Lehman, the Examiner would like to point out that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

The Examiner would also like to point out that the reference to Goldberg does not teach away from the possibility of combining Goldberg with Lehman to obtain the claimed invention as Goldberg's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton,* 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123. For example, Goldberg, in the Background section describes different methods for tracking and allocating available memory in a computer system wherein Goldberg explains that **["The use of multiple buffer pools allows storage resources to be allocated in a manner that conserves system resources. However, depending on the number of pools created within the system, more memory may still be allocated than is necessary... which results in a considerable waste of storage space" (col. 2, lines 26-35)]**; thus, contrary to Applicant's assertion, Goldberg is not criticizing, discrediting or discouraging the use of multiple buffer

pools for the allocation of available memory, but is merely explaining a specific situation in which more memory than is necessary is allocated using buffer pools, which results in waste of storage. Further, note that Goldberg is not criticizing, discrediting or discouraging the particular invention of Lehman or any modification resulting from combining Goldberg with Lehman, but is merely discussing particular solutions to a given problem that are alternate to the preferred embodiments of Goldberg.

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Goldberg and Lehman are involved and directed to memory access and control, more specifically, optimizing memory allocation by indicating available/unavailable memory wherein one of ordinary skill in the art would recognize that modifying Goldberg as taught by Lehman would provide the advantages of **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)]**, as taught by Lehman.

In view of the foregoing, the Examiner would like to accentuate that the combination of Goldberg and Lehman is proper and discloses the limitations required by the pending claims.

THIRD POINT OF ARGUMENT

27. In response to Applicant's argument that the combination of Goldberg and Lehman does not disclose "wherein the first state of the logic circuit comprises a number of available memory segments in the first memory block;" as Lehman teaches looking at the entire bit map to count up the number of "0" bits in the bit map. This argument has been fully considered; however, the Examiner respectfully disagrees.

28. It appears that Applicant is reading limitations not appearing in claimed language into the claims. The combination of Goldberg and Lehman discloses explicitly discloses "wherein the first state of the logic circuit comprises a number of available memory segments in the first memory block" as Lehman discloses **["The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided" (Col. 11, lines 6-14) wherein "blocks larger than 1 can start only on an appropriate block address… the bit string 1111 1100 0000 0011, represents one allocated block of size 4 (*which corresponds to a number of available memory segments in the first memory block comprised in the first state of the logic circuit which is represented by "0s;" the number of first state bits comprises a number of available memory segments in the first memory block*), one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text)]**; thereby disclosing the claimed limitation "wherein the first state of the logic circuit comprises a number of available memory segments in the first memory block."

29. Furthermore, there is not limitation in the claims distinguishing Applicant's invention from looking at the entire bit map to count up the number of "0" bits in the bit map since "0" bits represent "a first state" and these bits certainly "comprise a number of available segments in a

first memory block." Refer to **[bit string "1111 1100 0000 0011" having "0" bits in a first state which comprise a number of available memory segments in memory blocks; note two blocks having two "0" (*in a first state*) bits comprising two available segments and one block comprising four "0" bits comprising four available segments (Col. 11, lines 38-46) (Figure 7 and related text)]**; thereby disclosing a first state comprises a number of available segments in the first memory block.

FOURTH POINT OF ARGUMENT

30. Regarding Applicant's remark that the combination of Goldberg and Lehman does not disclose "wherein the second state of the first logic circuit comprises information indicating an offset to available memory" as the cited portions of Lehman teach pointer arrays to search for free blocks, which would teach away from the claimed invention and also argues "First, the Examiner interprets first logic circuit of Applicant's independent claim 13 to be a bit in a LLB as a disclosed in Goldberg… Then, the Examiner interprets the first logic circuit of Applicant's independent claim 13 to be a pointer array Lehman... Clearly, a bit in a LLB as disclosed in Goldberg is different than a pointer array as disclosed in Lehman. Thus, there is no motivation to combine features of a bit in a LLB with features of a pointer array."

In response, these arguments have been fully considered, but they are not deemed persuasive **[Refer to Second Point of Argument above for discussion regarding combination of Goldberg and Lehman]**.

The combination of Goldberg and Lehman discloses "wherein the second state of the first logic circuit comprises information indicating an offset to available memory" as Lehman discloses **["pointer array 124 permit the data manager to determine immediately if it**

should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text)]; therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory; disclosing a second state which comprises information indicating an offset to available memory.

In response, these arguments have been fully considered, but they are not deemed persuasive at least for the reasons stated in second point of argument above.

31. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated 12/8/2008.

Examiner's Note

32. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially

teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

33. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

34. Per the instant office action, claims 1-15 and 24-27 have received an on the merits and are subject of a final rejection.

a(2) CLAIMS REJECTED IN THE APPLICATION

35. Claims 16-23 and 28-40 stand canceled as of Applicant's submission filed on 12/8/2008.

b. DIRECTION OF FUTURE CORRESPONDENCES

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

37. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 3, 2009

/Yaima Campos/
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185